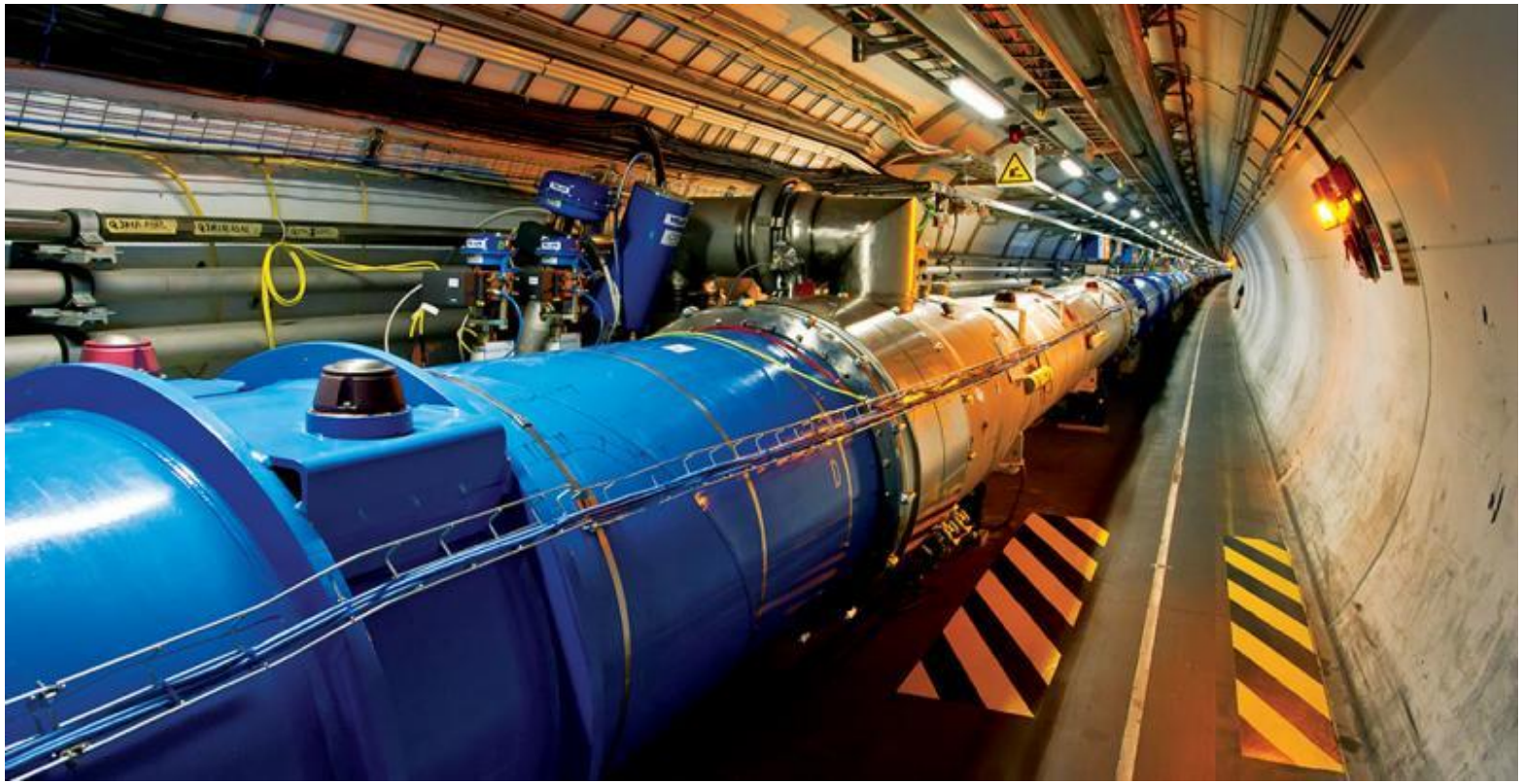


High DR ADC for LHC

Sarthak Kalani

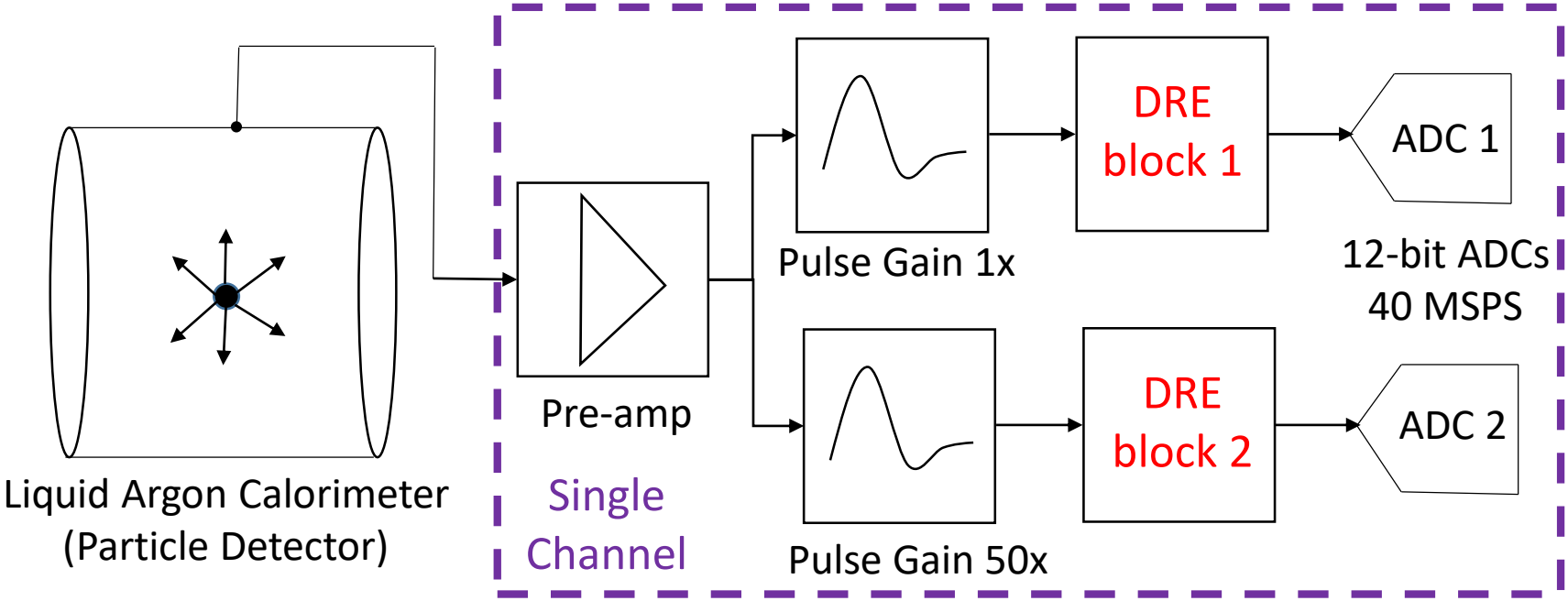
Last updated: 01/26/17

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

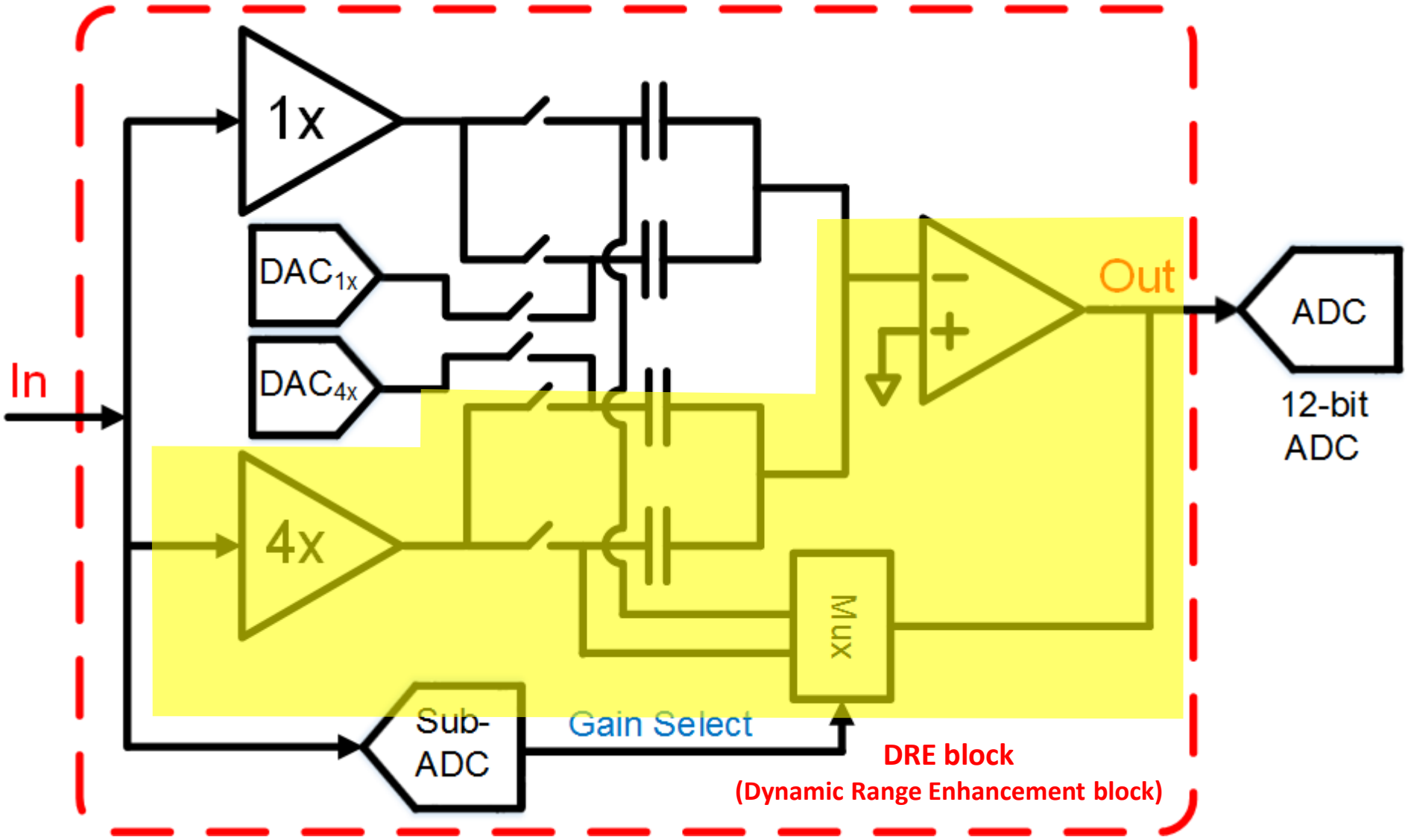
Columbia Integrated Systems Laboratory

Aim: ADC design for The LHC (Large Hadron Collider), CERN

- ADC specifications:
  - 14-bit design: To accommodate high dynamic range (16 bit)
  - 40MSps
- To design: intermediate block
  - Increase accuracy to 14 bit (or enhance the dynamic range)



Previously: 4x Branch simulation

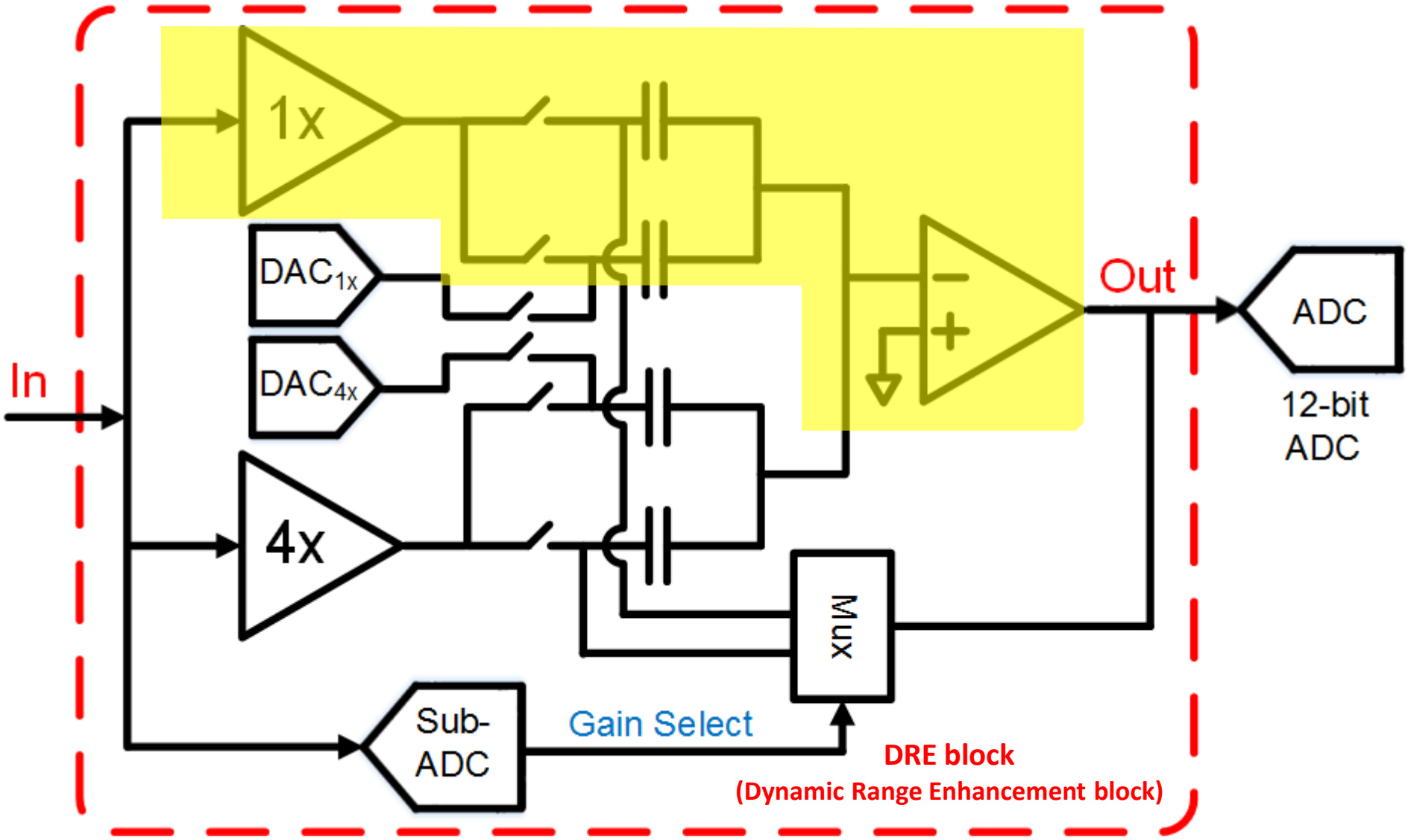


Previous results:
4x branch@ 5MHz Input, 40MSPS

- Simulations contain:
  - Transistor level transient simulation
  - Transient noise enabled
- Tt, ff, ss, sf and fs corners simulated for 0°C and 50°C
  - Worst case (ss0) limited by both noise and distortion

Corner	SNR (dB)	SDR (dB)	SNDR (dB)	Power (mW)	$Vout_{pp}$ (diff) (V)
tt 0	63.0	68.5	62.0	108	1.6
tt 50	62.3	74.0	62.0	111	1.6
ss 0 (worst THD)	63.3	64.8	61.1	86	1.6
ff 50	62.4	82.7	62.4	121	1.6

1x Branch simulation

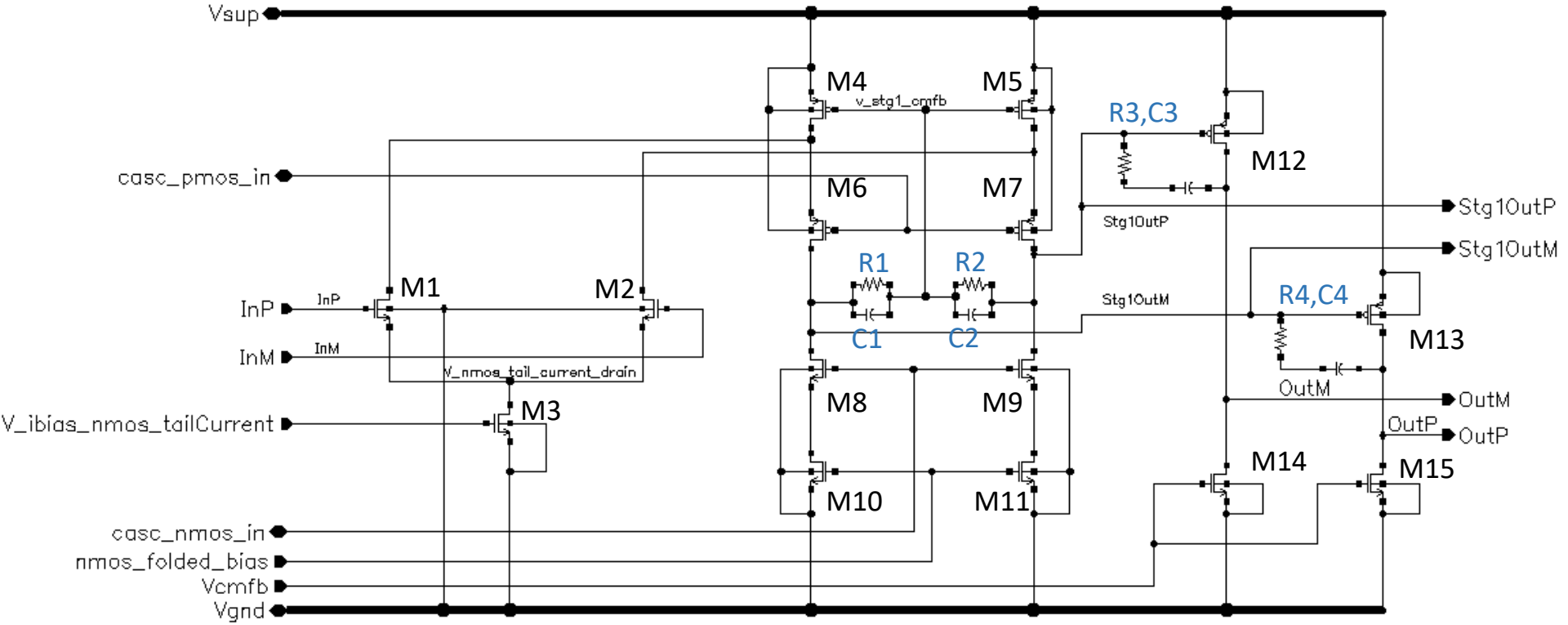


1xbranch result @ 5MHz Input, 40MSPS

- Simulations contain:
  - Transistor level transient simulation
  - Transient noise enabled
- Only ss 0^{o}C simulated (worst case for SDR)
- Obtained SNDR of 61dB (similar to 4x branch)

Important: Transistor sizes!

Transistor level differential amplifier



M1,M2 = 1920u/240n

M3 = 1280u/240n

M4,M5 = 3840u/240n

M6, M7 = 5760u/240n

M8,M9 = 1920u/240n

M10, M11 = 640u/240n

M12,M13 = 1920u/240n

M14,M15 = 640u/240n

R1,R2 = 200kΩ

R3,R4 = 0(zero)Ω

C1,C2 = 1pF

C3,C4 = 14pF

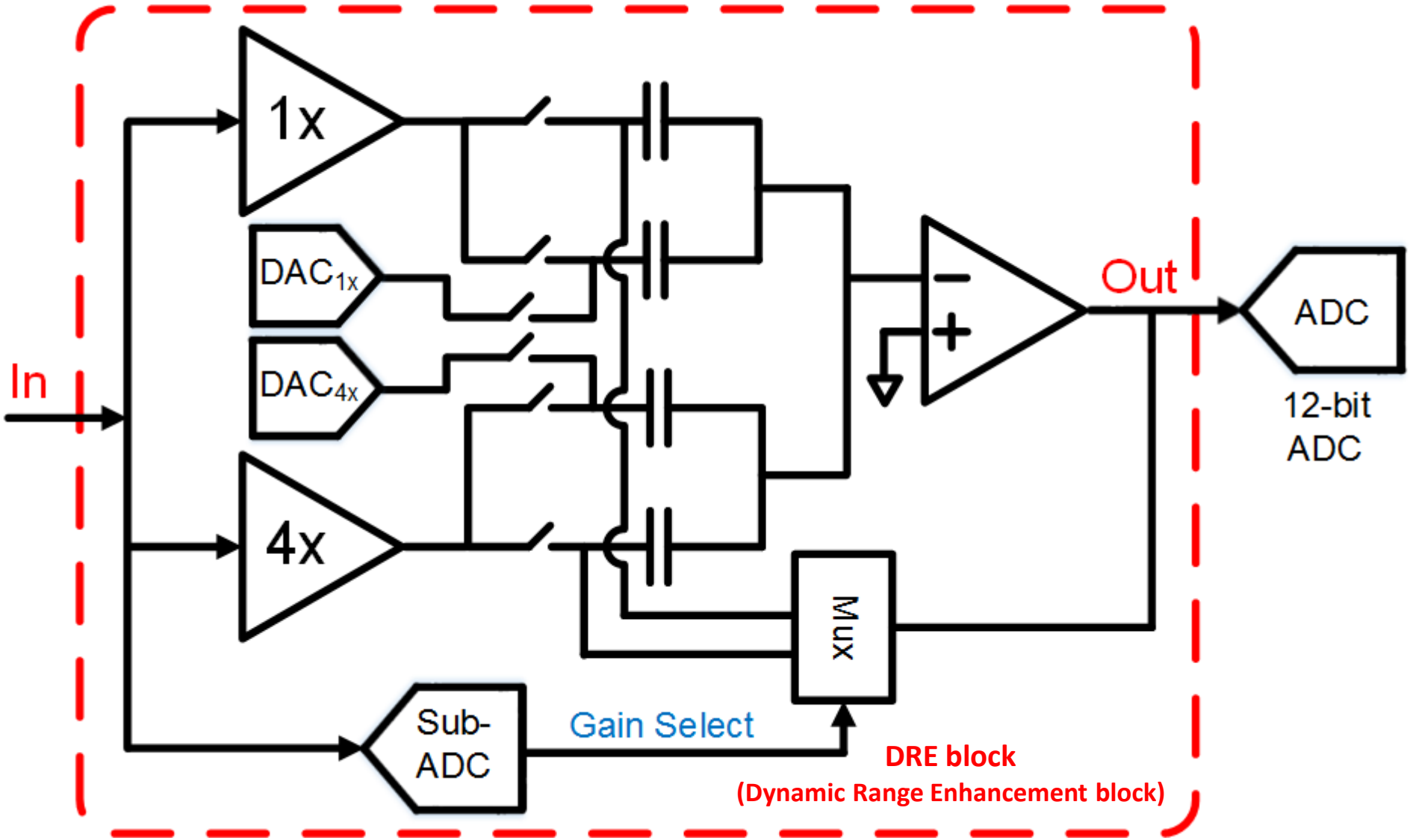
W/L = 16,000

Cload = 4pF

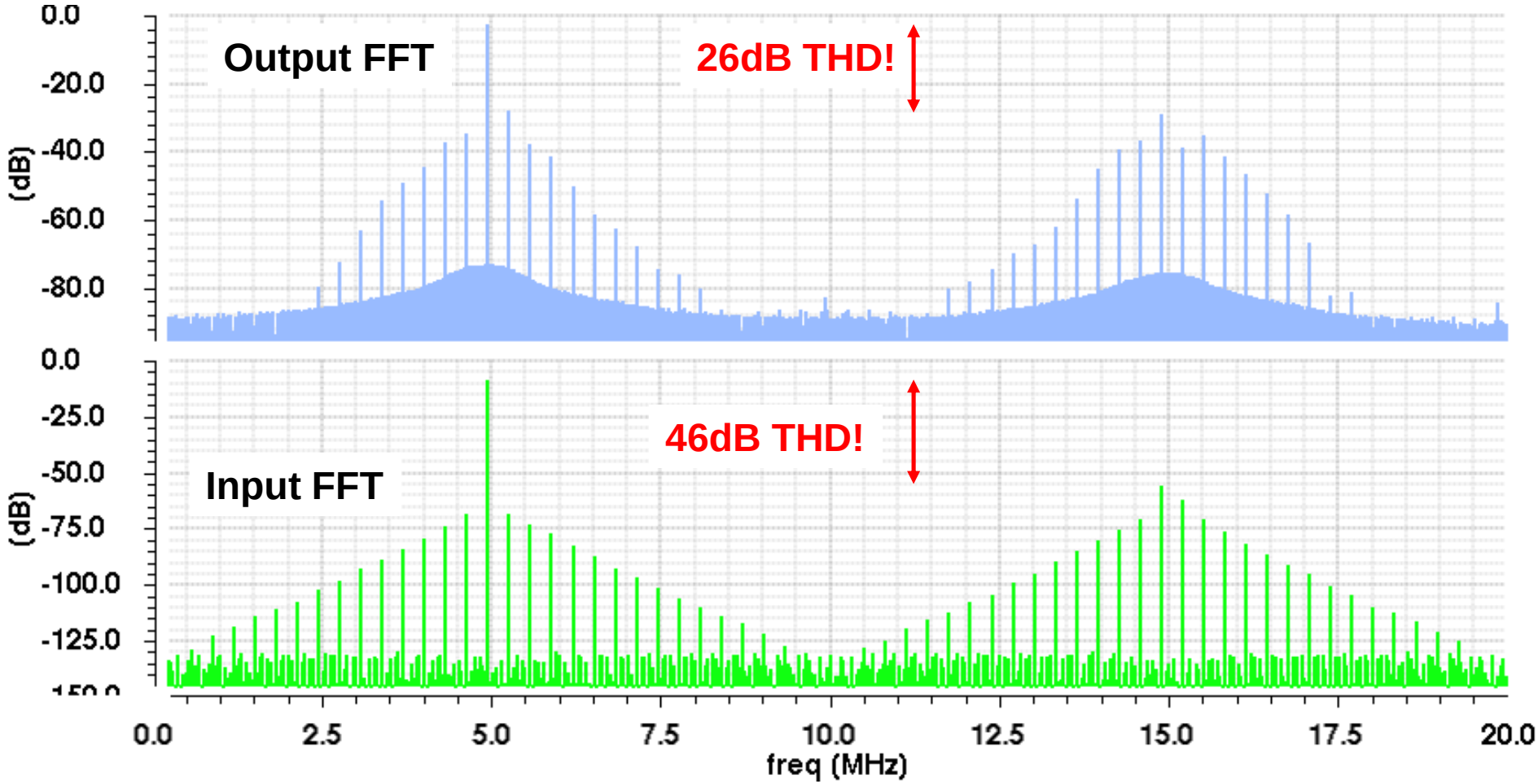
Discussion: Large transistor sizes

- Necessary because RVT devices used currently:
  - Differential input pair: 600mV common mode.
  - V_{th} = 550mV for worst corner.
  - Need to go in weak inversion, using large sizes
  - Large current additionally necessitates huge transistor sizes
- Current plan:
  - Complete 1st version at system level with current design (large transistors)
- Plan for 2nd version of the design:
  - Use of LVT devices, V_{th} is 426mV for worst corner.
  - Smaller transistor size is expected, though devices will still be relatively large

Combined branch simulation



Output for 1x branch corrupted!



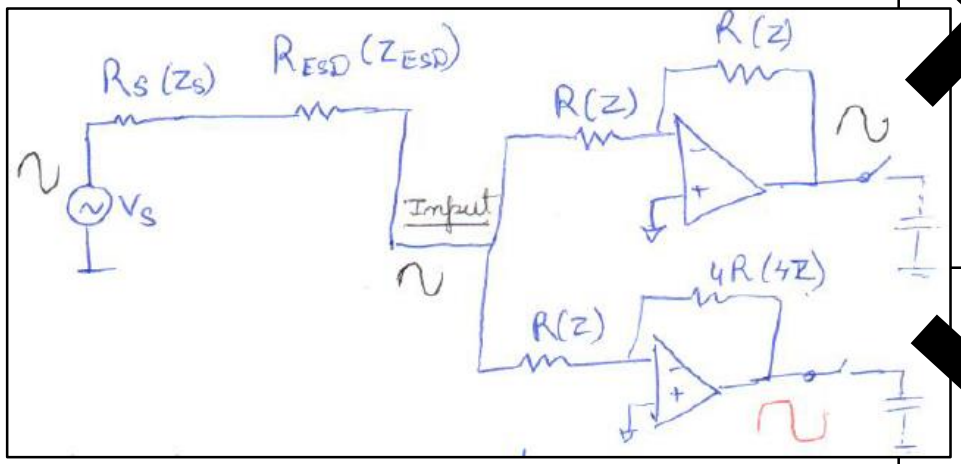
1x branch selected for combined 1x and 4x branch schematic.
Fin = 127/1024*Fs, Input Amplitude = 0.4V

Reason: Strong non-linearity from 4x branch

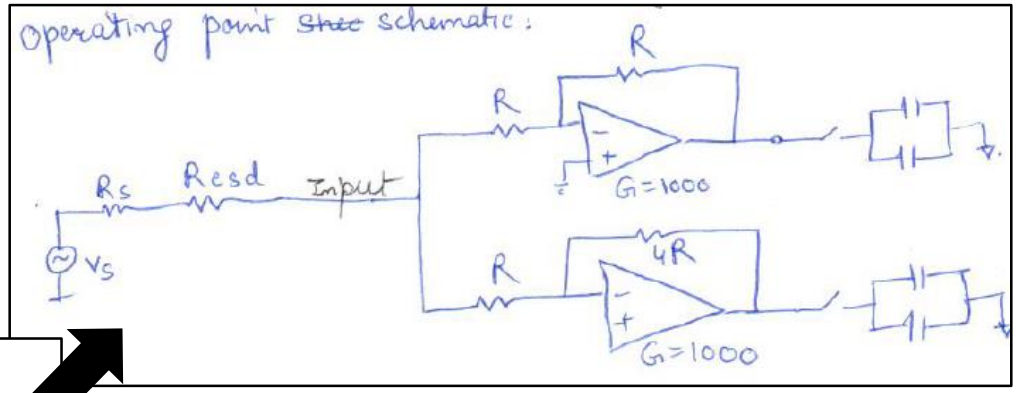
$$V_{nl,in} = \frac{V_{nl,out} * ((R_{esd}+R_{in})||R)}{4R}$$

$$\Rightarrow \boxed{V_{nl,in} \approx \frac{V_{nl,out}}{20}}$$

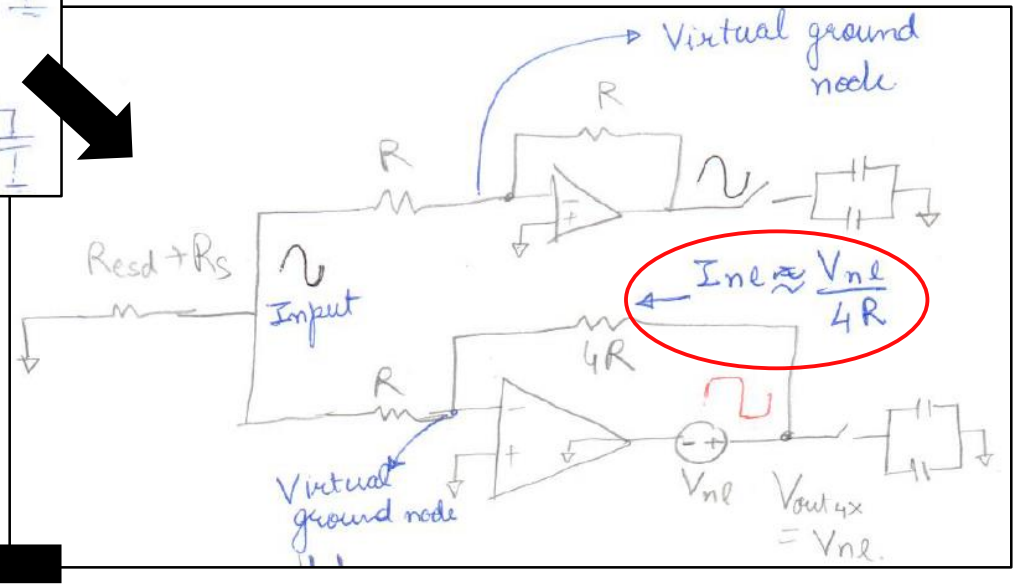
Main Circuit



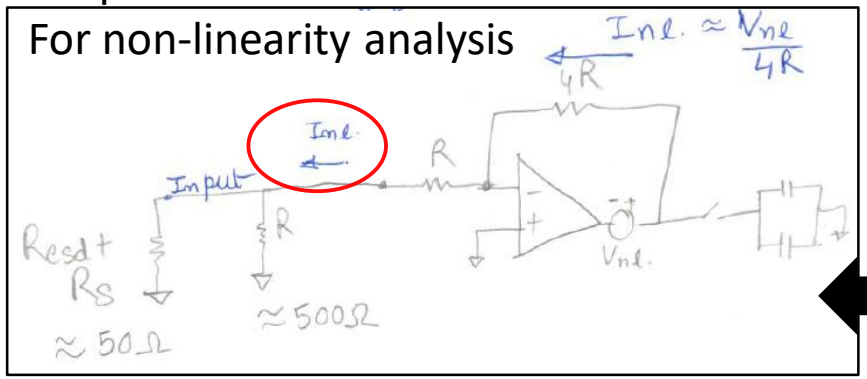
Operating point analysis



Non-linearity analysis

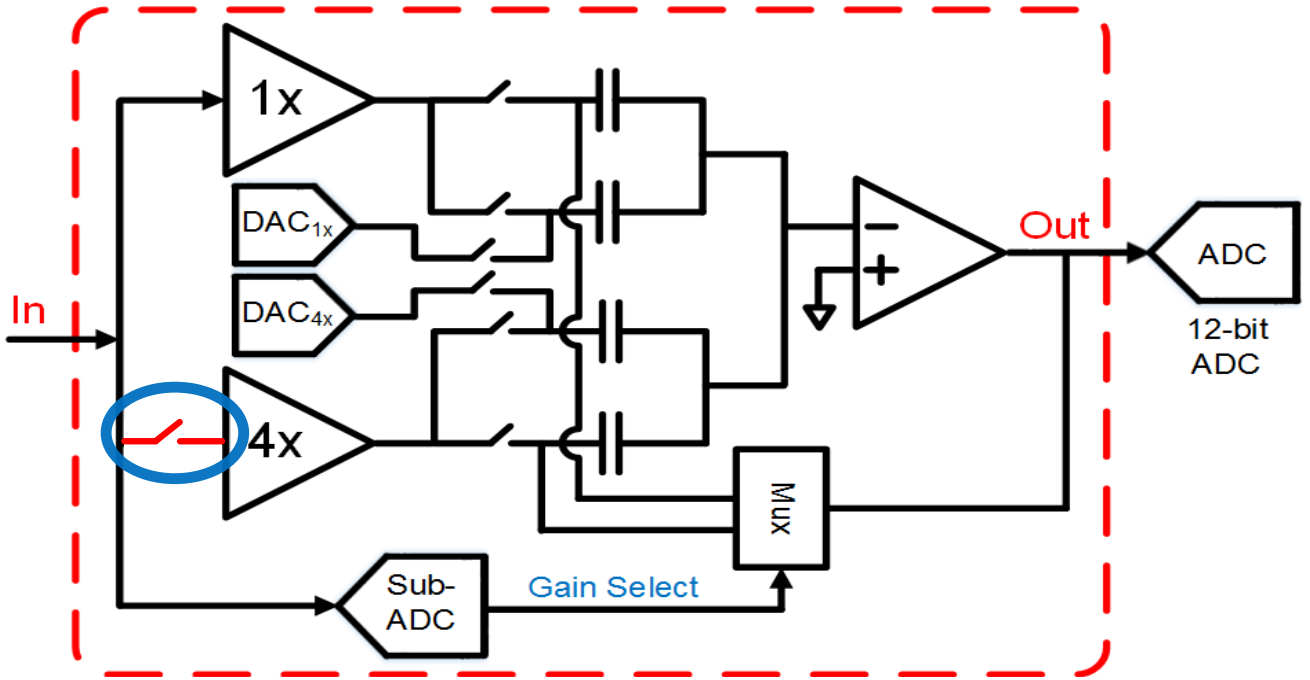


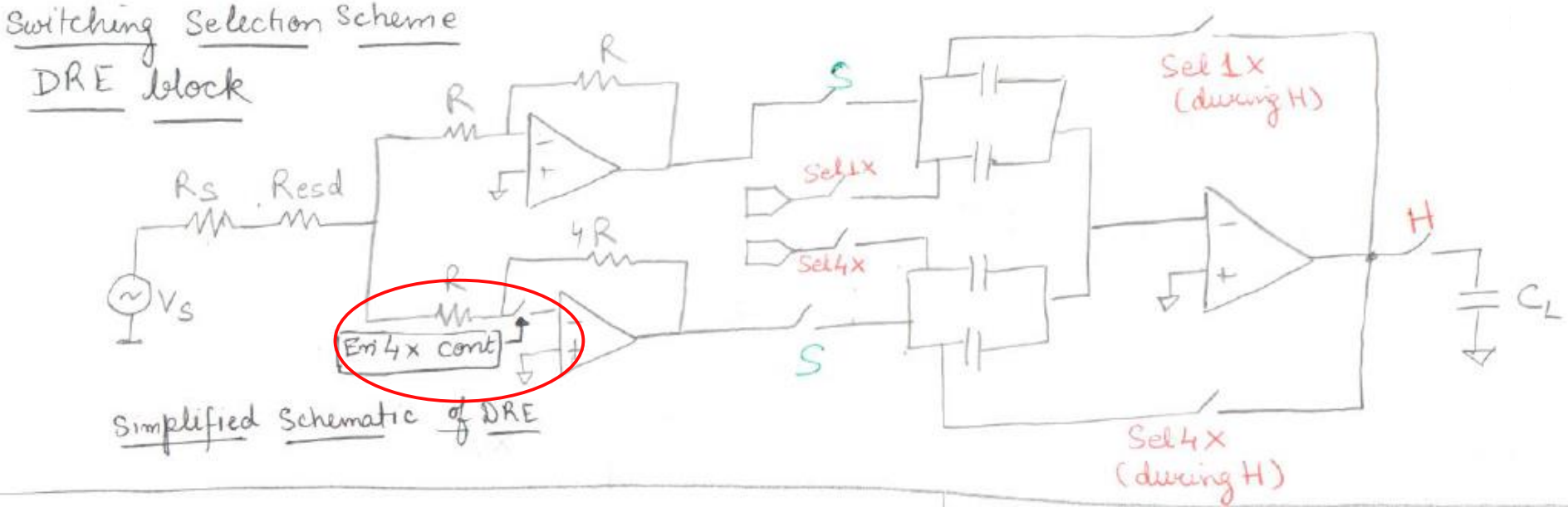
Simplified schematic
For non-linearity analysis



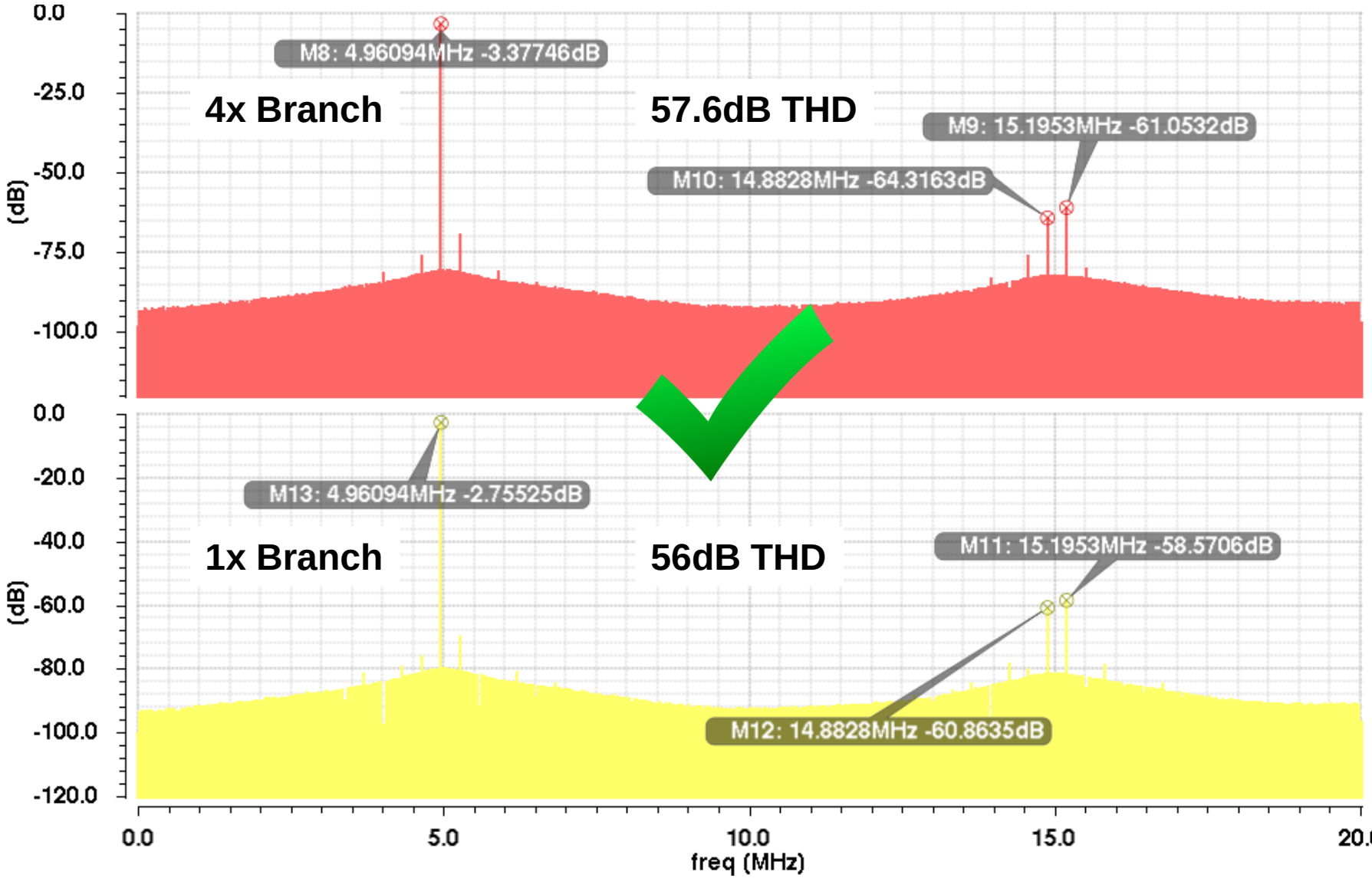
Proposed improvement

Introduce switch for 4x branch

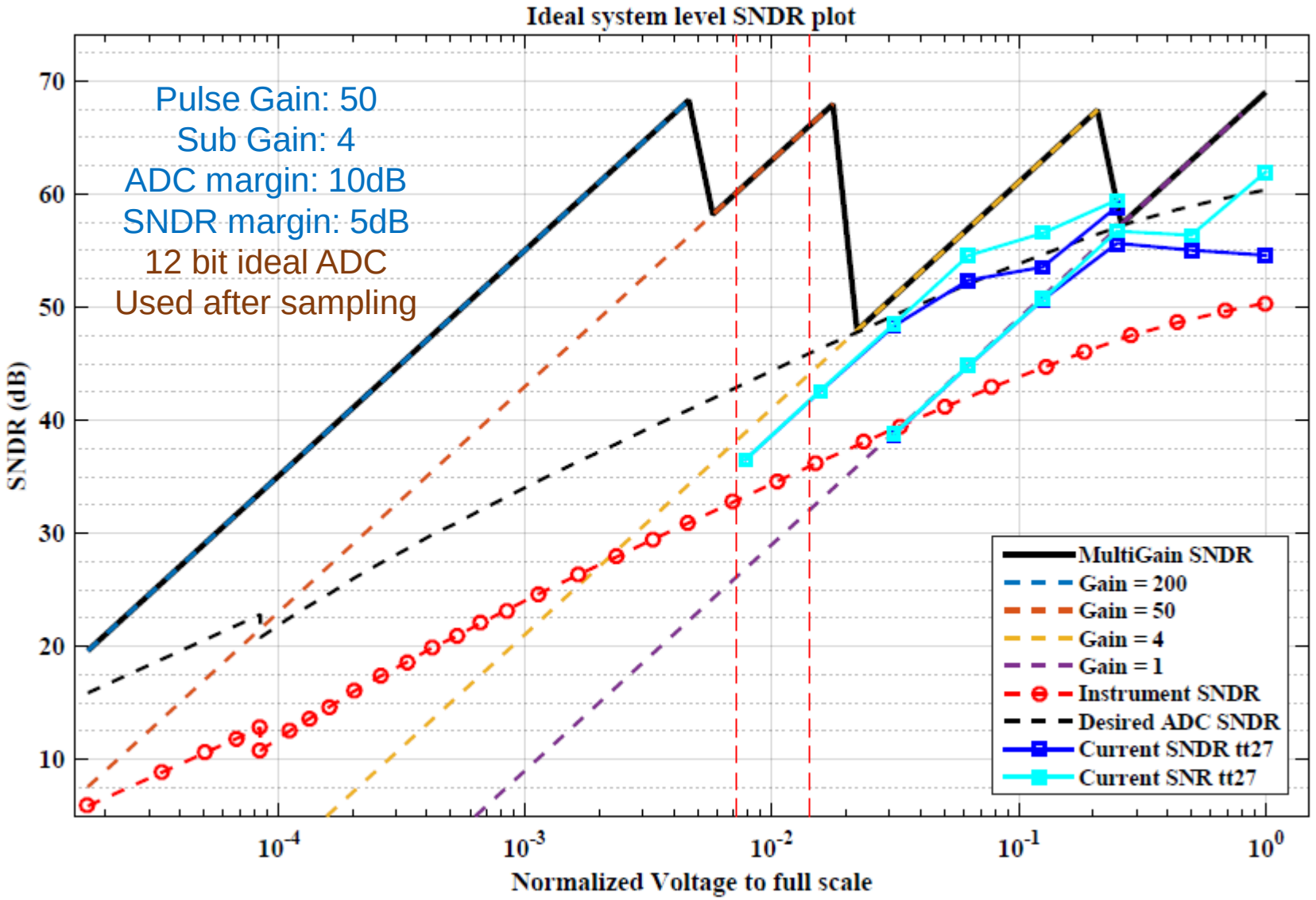




Simulation results (ss 0^0C, transistor level, 5MHz input)



Current status on SNDR curve



DRE input requirements: Updated

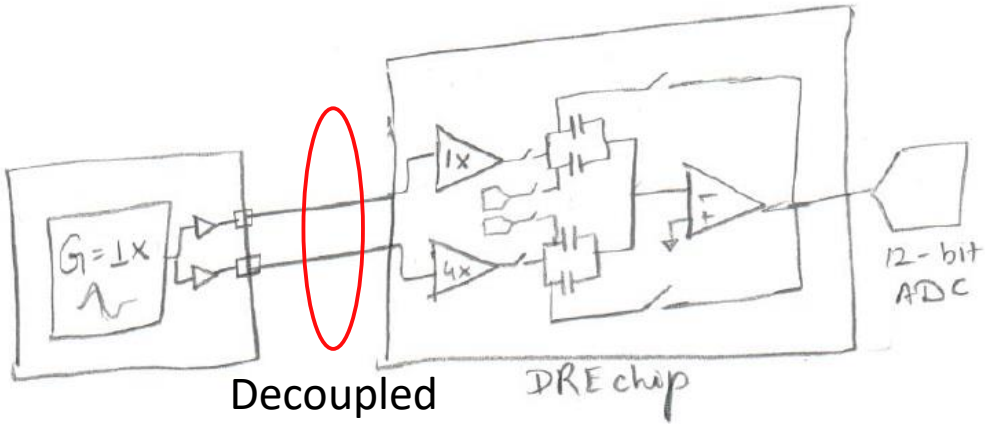
Previously:

Requirement	Value
Input Resistance to be driven	250Ω single ended (1x and 4x branch having 500Ω each)
Input Capacitance to be driven	17pF Single ended (8pF each for 1x and 4x branch and 1pF for Sampling ADC)
Vpp differential input	1.6V

Additionally:

Can we have two decoupled outputs from previous interface chip?

This will greatly simplify 1x and 4x coupling challenges



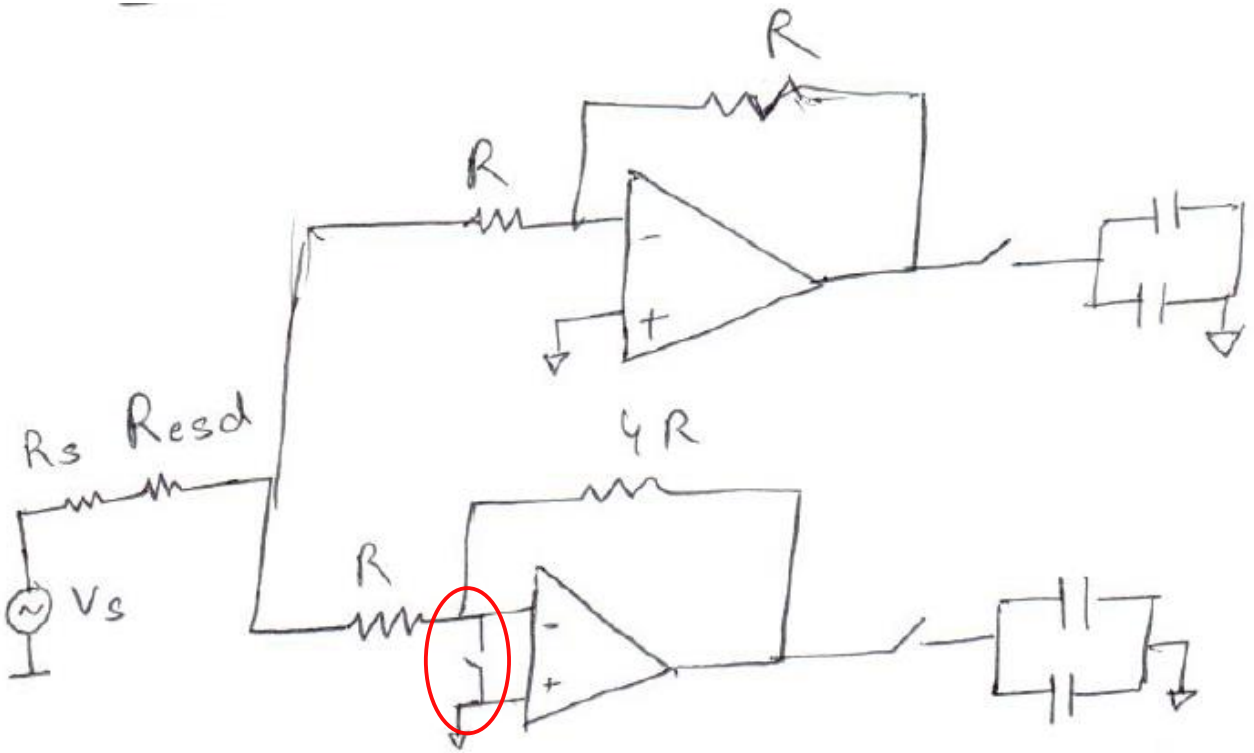
Future plans

- Implement automatic gain selection mechanism.
- Start with LVT version of amplifier.

- Chip tapeout plans:
  - Chip 1: Only DRE block
    - Area estimate: 1mm x 1mm
  - Chip 2: DRE + 12 bit ADC (combined with UT-A)
    - Inner area estimate (without pads): 0.5mm x 0.8mm

Backup slides

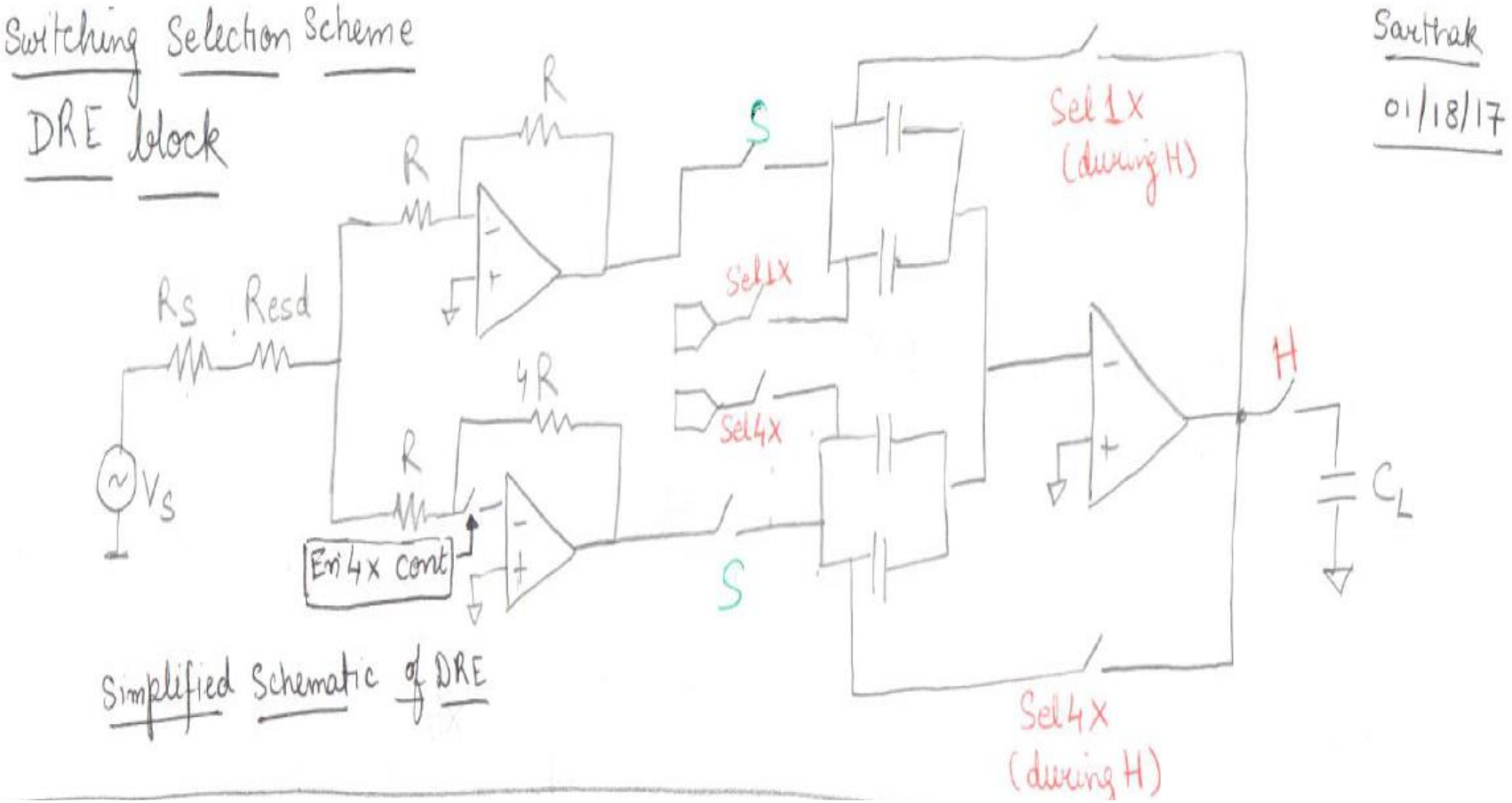
Alternate switch position for 4x branch



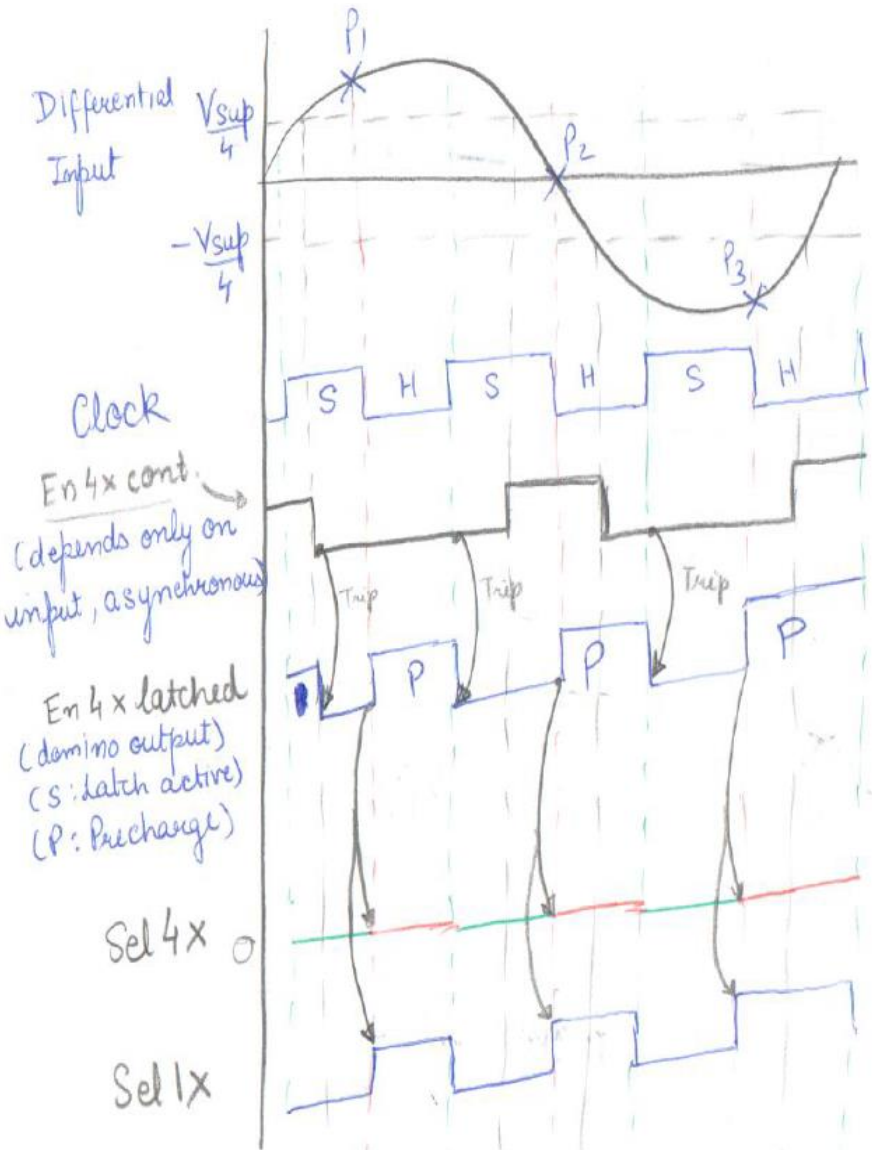
Benefit: Unlike previous version, common mode settling is not required

Verification still in progress.

Switching selection scheme



Switching selection scheme (contd.)



Timing

→ S ⇒ 1x & 4x Sample

→ Hadv ⇒ Decide 1x or 4x

→ H ⇒ Either Sel 1x or Sel 4x becomes 1.

Selection process:

→ H ⇒ Precharge (P) En4x latched node (output of domino latch)

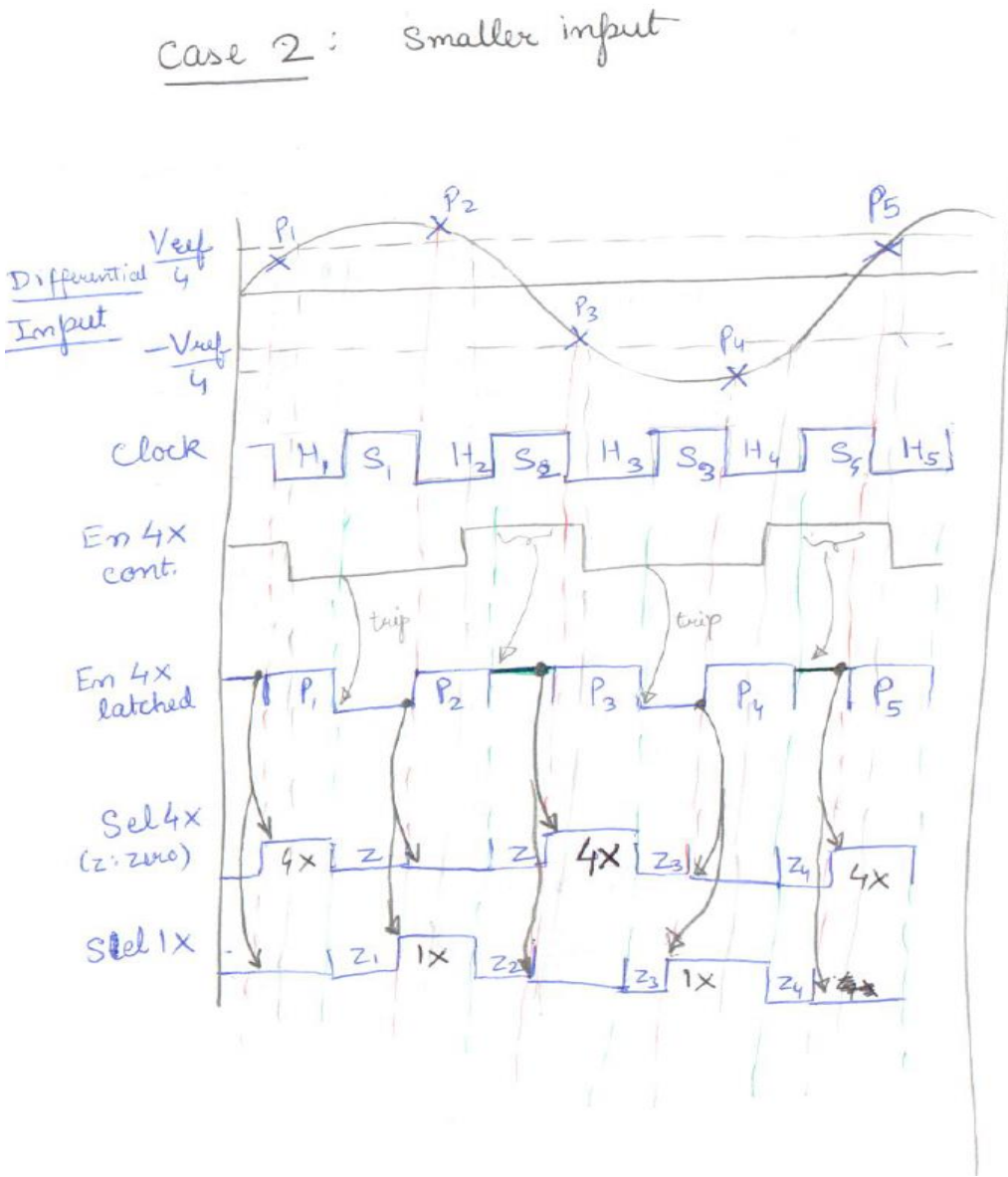
→ S ⇒ Latch active, anytime En4x cont is 0 (zero), domino trips, output 0.

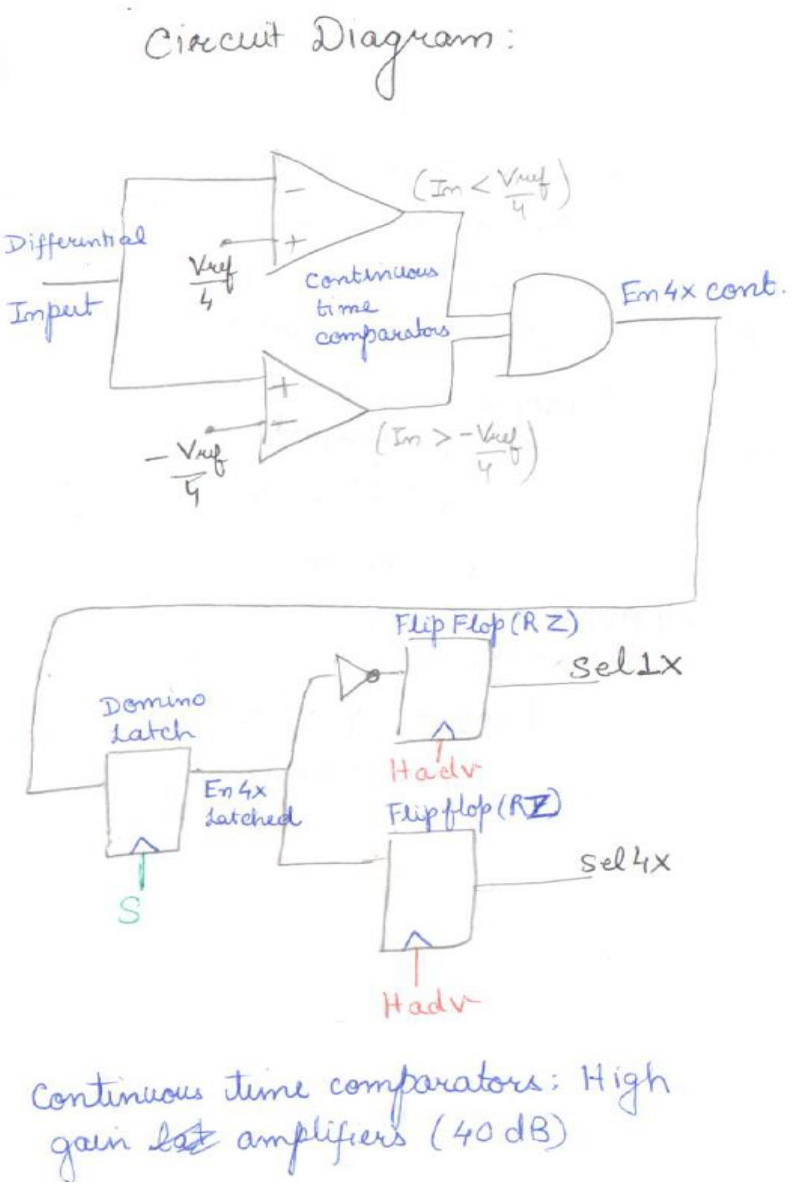
→ H adv ⇒ Transfer latch value to make either sel 1x active or Sel 4x active

→ H ⇒ cycle repeats

→ During S, sel 1x & sel 4x are 0 (zero)

Switching selection scheme (contd.)

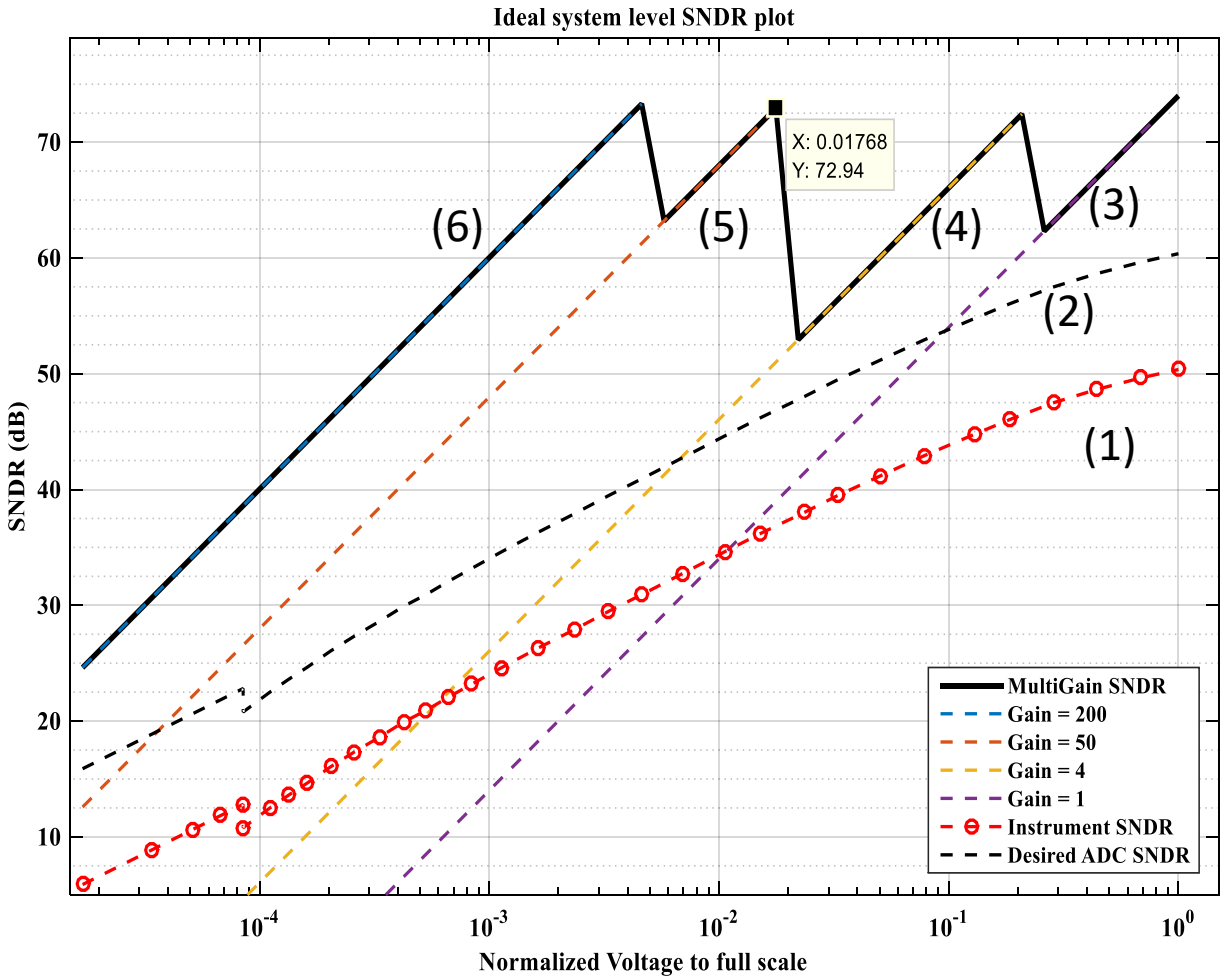




System level SNDR requirements

- 1-bit provided by sample stage MDAC
- 11-bit ADC is expected to provide 67.7dB SNDR
- Overall 12-bit ADC requirement of 73dB obtained by combination of 1-bit output and 11-bit ADC

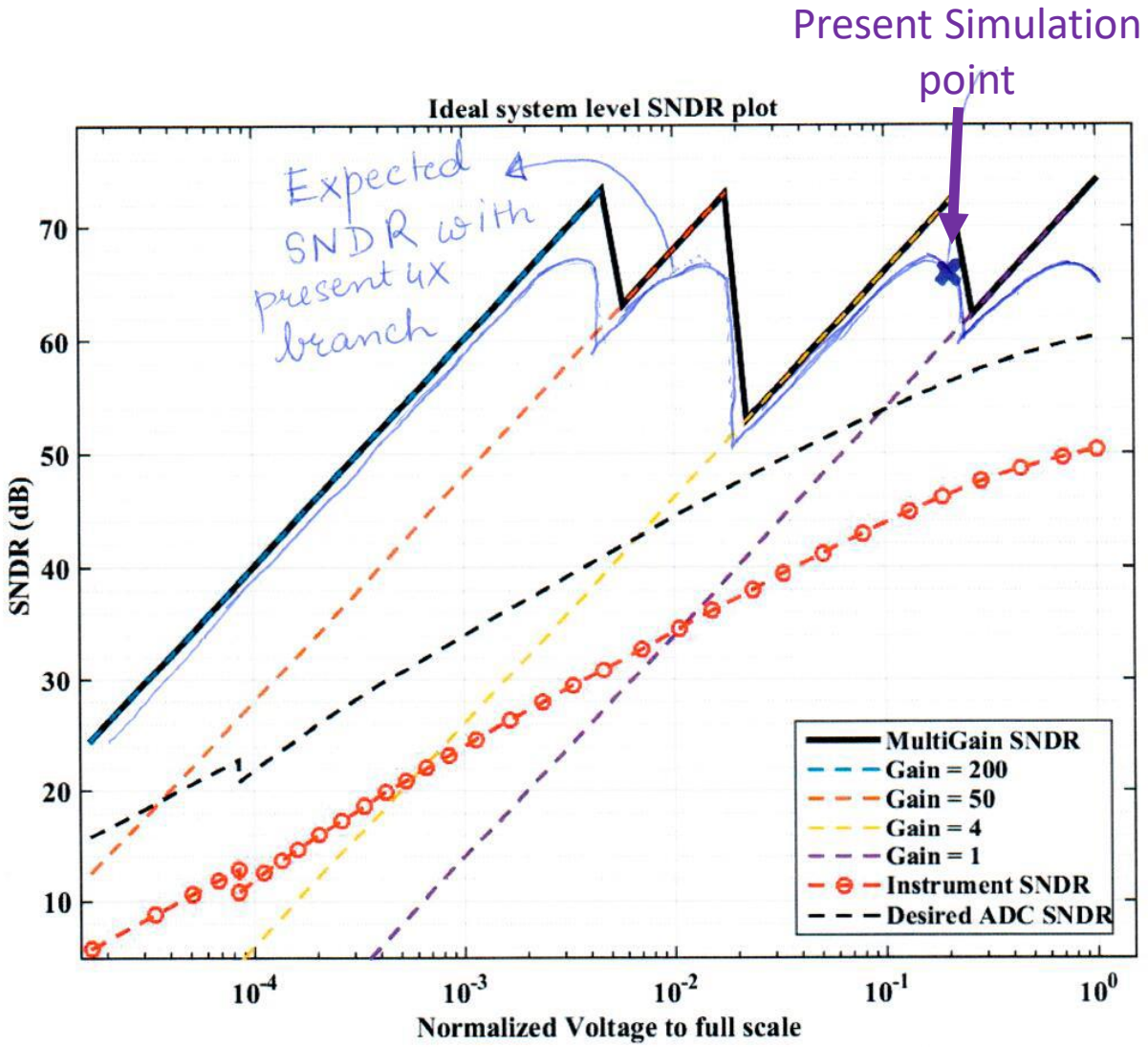
- Ideally need 67dB SNDR at the MDAC output.
- Currently worst case SNDR is 61dB.



System level requirements satisfied!

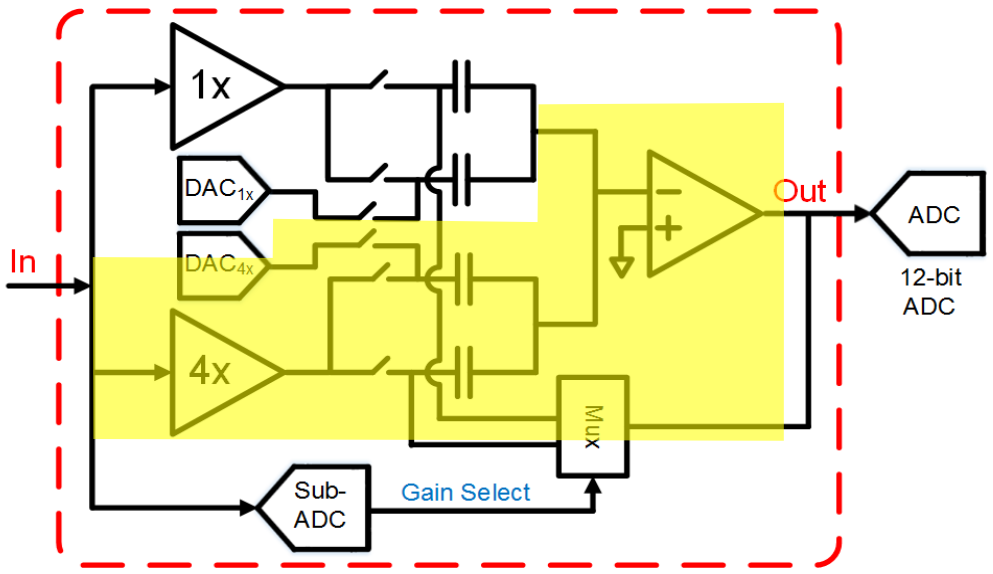
- 1-bit provided by sample stage MDAC
- 61.1 dB SNDR obtained in the worst case simulation
- After combining, SNDR obtained is 67.1dB

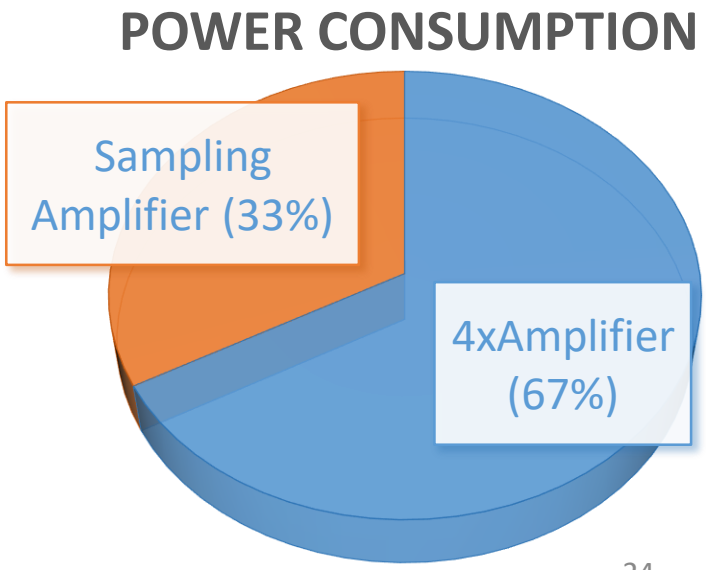
- Overall system level requirements are still satisfied



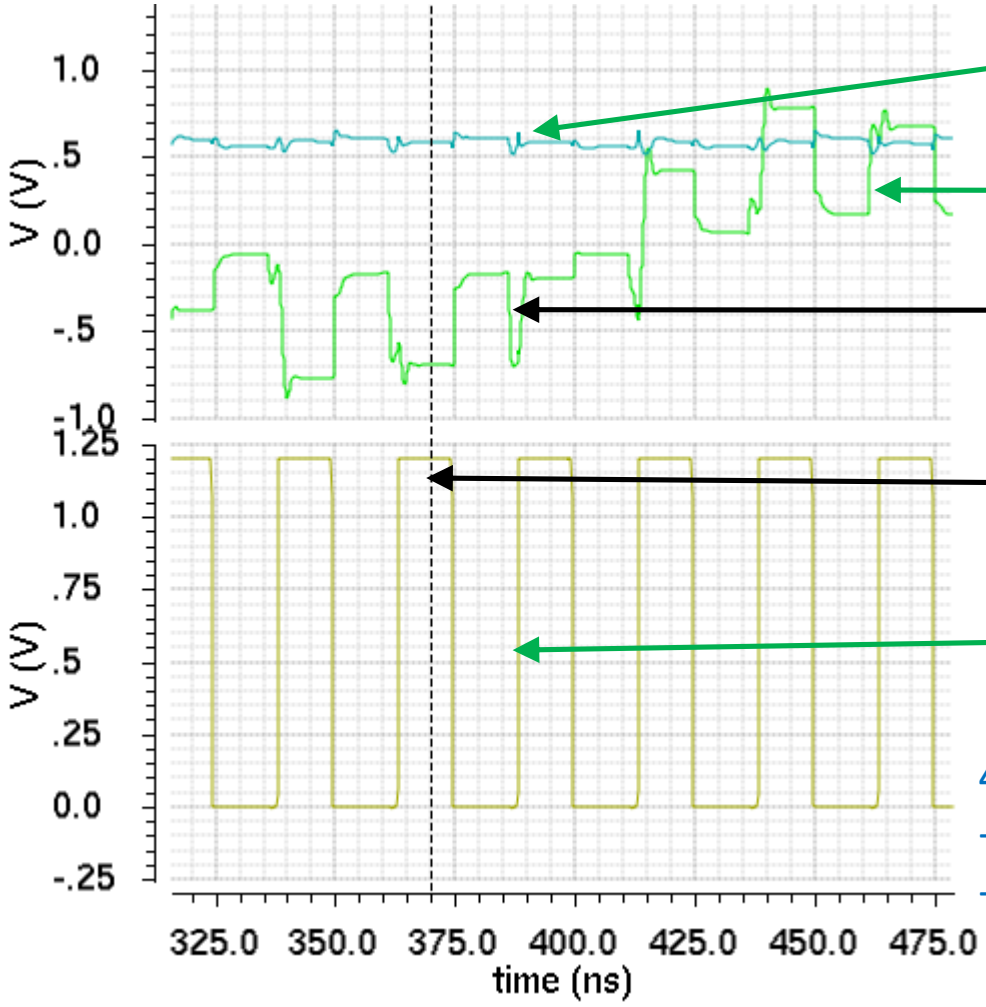
Power consumption for 4x branch

- For ss 0°C case:
  - Total power = 86mW
  - 4x Amplifier power = 58mW (67%)
  - Sampling Amplifier power = mW (33%)
- Power required in 4x Amplifier to increase SNR





Sampled output waveform



Output Common Mode

Differential Output

Sample and hold clock non-overlap period

Value settled by the end of hold clock

Hold clock

4x branch transistor level simulation for:
- 0.1V input amplitude (8x gain at output)
- tt 0°C corner